WHAT IS CLAIMED IS:

1. A non-volatile memory cell comprising:

a substantially single crystalline substrate of a first conductivity type having a planar surface;

a trench in said planar surface, said trench having a side wall and a bottom;

a floating gate in said trench spaced apart and insulated from said sidewall and from said bottom; said floating gate having a tip away from said bottom;

a first region of a second conductivity type in said bottom;

a second region of a second conductivity type along said planar surface, spaced apart from said first region;

a channel region between said first region and said second region, said channel region along said sidewall;

a control gate capacitively coupled to said floating gate and capable of effecting erase; and

a tunnel material between said tip and said control gate.

2. The memory cell of claim 1 wherein said tunnel material is a tunnel oxide.

3. The memory cell of claim 2 wherein said tunnel oxide permits Fowler-Nordheim tunneling of charges from said floating gate to said control gate.

4. The memory cell of claim 1 further comprising an insulation material between said floating gate and said sidewall of said trench, said insulation material permitting injection of hot channel electrons from said channel region to said floating gate.

5. An array of non-volatile memory cells in a substantially single crystalline substrate of a first conductivity type having a planar surface, said array comprising:

a plurality of discontinuous trenches in said planar surface, spaced apart and substantially parallel to one another extending in a first direction; each of said discontinuous trenches having two sidewalls and a bottom and being discontinuous in said first direction by a plurality of isolations;

a first floating gate in each trench spaced apart and insulated from a first sidewall and from said bottom; said first floating gate having a tip away from said bottom;

a second floating gate in each trench spaced apart and insulated from a second sidewall and from said bottom; said second floating gate having a tip away from said bottom;

a first region of a second conductivity type in said bottom of each trench;

a second region of said second conductivity type along said planar surface;

a channel region between each of said first region and said second region, said channel region along said first and second sidewall;

a plurality of control gates, each control gate extending in a second direction, substantially perpendicular to said first direction, extending over a plurality of tips of a plurality of floating gates and insulated therefrom; and

a tunnel material between said plurality of tips and said control gate.

6. The array of claim 5 wherein said tunnel material is a tunnel oxide.

7. The array of claim 6 wherein said tunnel oxide permits Fowler-Nordheim tunneling of charges from said floating gates to said control gate.

8. The array of claim 5 further comprising an insulation material between said first floating gate and said first sidewall of said trench, said insulation material permitting injection of hot channel electrons from said channel region to said first floating gate.

9. The array of claim 8 further comprising said insulation material between said second floating gate and said first sidewall of said trench, said insulation material permitting injection of hot channel electrons from said channel region to said second floating gate.

10. A non-volatile memory device in a substantially single crystalline substrate of a first conductivity type having a planar surface, said device comprising:

an array of non-volatile memory cells arranged in a plurality of rows and columns; wherein each cell comprising:

a trench in said planar surface, said trench having a side wall and a bottom;

a floating gate in said trench spaced apart and insulated from said sidewall and from said bottom; said floating gate having a tip away from said bottom;

a first region of a second conductivity type in said bottom;

a second region of a second conductivity type along said planar surface, spaced apart from said first region;

a channel region between said first region and said second region, said channel region along said sidewall;

a control gate spaced apart from said tip and capacitively coupled to said tip; and

a tunnel material between said tip and said control gate; and

wherein cells in adjacent columns share a common trench to one side and a common second region to another side;

wherein cells in adjacent rows are separated by an isolation row and wherein said second region in one row is connected to said second region of another row; and;

wherein said control gate of cells in the same row are connected together.

11. The device of claim 10 wherein a control gate extends over a plurality of rows.

12. The array of claim 11 wherein said tunnel material is a tunnel oxide.

13. The array of claim 12 wherein said tunnel oxide permits Fowler-Nordheim tunneling of charges from said floating gates to said control gate.

14. The array of claim 11 further comprising an insulation material between said first floating gate and said first sidewall of said trench, said insulation material permitting injection of hot channel electrons from said channel region to said first floating gate.

15. The array of claim 14 further comprising said insulation material between said second floating gate and said first sidewall of said trench, said insulation material permitting injection of hot channel electrons from said channel region to said second floating gate.

16. A NAND circuit device comprising:

a plurality of stacked gate non-volatile memory cells arranged in a plurality of rows and columns; each cell having a first terminal and second terminal with a channel region therebetween, a floating gate spaced apart and insulated from said channel region, and a control gate capacitively coupled with said floating gate to effect erasure;

wherein said cells in the same row are connected with each cell having a common second terminal with an adjacent cell to one side, and having a common first terminal with an adjacent cell to another side;

wherein cells in the same row have the control gate connected together; and

wherein cells in adjacent rows are separated by isolation.

17. The device of claim 16 wherein said first terminal is in a trench and said second terminal is not in a trench.

18. The device of claim 16 wherein said floating gate of cells in the same row are capacitively coupled to the same control gate.

19. The device of claim 16 wherein cells in the same column have the same first terminal and the same second terminal.

20. A method of operating a stacked gate non-volatile memory cell having a first terminal, a second terminal with a channel region therebetween, a floating gate spaced apart and insulated from said channel region, and a control gate insulated from said floating gate and capacitively coupled thereto, said method comprising:

programming said cell by supplying a first voltage to said second terminal, supplying a second voltage, more positive than said first voltage, to said control gate, causing electrons from said second terminal to be injected onto said floating gate;

reading said cell by supplying a third voltage to said control gate, a fourth voltage to said second terminal, different from said third voltage, and determining the current flow between said first and second terminals; and

erasing said cell by supplying a fifth voltage to said control gate, a sixth voltage to

said first terminal, causing electrons from said floating gate to Fowler-Nordheim tunnel to said control gate.

21. A method of manufacturing an array of non-volatile memory cells in a substantially single crystalline substrate of a first conductivity type having a planar surface, said method comprising:

forming a plurality of trenches in said planar surface, spaced apart from one another, and substantially parallel to one another in a first direction; each of said trenches having two sidewalls and a bottom with spaced apart isolation regions in said trench;

forming a first region of a second conductivity type in said bottom of each of said trenches;

forming a second region of a second conductivity type on said planar surface between each trench;

forming a floating gate on each of said first and second sidewalls adjacent thereto and spaced apart and insulated therefrom and from said bottom; each floating gate having an end away from said bottom;

forming a tunnel material about said end;

forming a control gate on said tunnel material, substantially parallel to one another in a second direction substantially perpendicular to said first direction;and

forming a contact to said first and second regions.

22. The method of claim 21 wherein said first region and second region are formed by ion implantation.

23. The method of claim 22 wherein said contact to said first region is formed through said control gate.

24. The method of claim 22 wherein said contact to said second region is formed through said control gate.